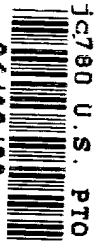
07-05-00 A



Please type a plus sign (+) inside this box [+]

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 042390.P8839 Total Pages 2

First Named Inventor or Application Identifier Brian K. Holscher

Express Mail Label No. EL 431686995US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 15)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 3)

4. X Oath or Declaration (Total Pages 5)

a. X Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ___ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ___ Microfiche Computer Program (Appendix)

7. __ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
__X__ b. Power of Attorney (signed)
10. _____ English Translation Document (if applicable)
11. _____ a. Information Disclosure Statement (IDS)/PTO-1449
_____ b. Copies of IDS Citations
12. _____ Preliminary Amendment
13. __X__ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. __X__ Other: separate sheet with title, express mail label, copy of postcard and attorney's signature

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
___ Continuation ____ Divisional ____ Continuation-in-part (CIP)
of prior application No: __

18. **Correspondence Address**
_____ Customer Number or Bar Code Label _____ (Insert Customer No. or Attach Bar Code Label here)
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Our Reference: 042390.P8839 *Patent*

BUFFER ALLOCATION CIRCUIT

Inventors: Brian K. Holscher

Respectfully submitted,

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"Express Mail" mailing label number: EL 431686995US
Date of Deposit: June 30, 2000
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(Signature of person mailing paper or fee) (Date signed)

Serial/Patent No.: **Not Yet Assigned** Filing/Issue Date: **Herewith**
Client: **Intel Corporation**
Title: **BUFFER ALLOCATION CIRCUIT**

BSTZ File No.: **042390.P8839** Atty/Secty Initials: **RAB/dcv**
Date Mailed: **June 30, 2000** Docket Due Date:

The following has been received in the U.S. Patent & Trademark Office on the date stamped hereon:

- ☐ Amendment/Response (____ pgs.)
- ☐ Appeal Brief (____ pgs.) (in triplicate)
- ■ Application - Utility (15 pgs., with cover and abstract)
- ☐ Application - Rule 1.53(b) Continuation (____ pgs.)
- ☐ Application - Rule 1.53(b) Divisional (____ pgs.)
- ☐ Application - Rule 1.53(b) CIP (____ pgs.)
- ☐ Application - Rule 1.53(d) CPA Transmittal (____ pgs.)
- ☐ Application - Design (____ pgs.)
- ☐ Application - PCT (____ pgs.)
- ☐ Application - Provisional (____ pgs.)
- ■ Assignment and Cover Sheet **(signed)**
- ■ Certificate of Mailing
- ■ Declaration & POA (5 pgs.) **(signed)**
- ☐ Disclosure Docs & Orig & Copy of Inventor's Signed Letter(____pgs)
- ■ Drawings: 3 # of sheets includes 5 figures
- ■ Express Mail No. **EL431686995US** ■ Check No. **000541**
- ☐ ____ Month(s) Extension of Time Amt: **$730.00**
- ☐ Information Disclosure Statement & PTO-1449 (__ pgs.) ☐ Check No.____
- ☐ Issue Fee Transmittal Amt: ____
- ☐ Notice of Appeal
- ☐ Petition for Extension of Time
- ☐ Petition for ____
- ■ Postcard
- ☐ Power of Attorney (____ pgs.)
- ☐ Preliminary Amendment (____ pgs.)
- ☐ Reply Brief (____ pgs.)
- ☐ Response to Notice of Missing Parts
- ☐ Small Entity Declaration for Indep. Inventor/Small Business
- ■ Transmittal ~~XXX~~ in duplicate **(2 pgs)**
- ■ Fee Transmittal, in duplicate **(2 pgs)**

■ Other: **Certificate of mailing with copy of return postcard signed by attorney**

Attorney Docket: 042390.P8836

APPLICATION FOR UNITED STATES LETTERS OF PATENT

FOR

BUFFER ALLOCATION CIRCUIT

Inventor(s): **BRIAN K. HOLSCHER**

Prepared by:

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MINIMUM GATE COUNT BUFFER ALLOCATION CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally concerns buffer allocation in processing devices, and in particular concerns allocation of a next available buffer in a microprocessor.

2. Background Information

A common approach in trying to find the next available buffer in a processing device is to implement priority encoders, which determine the next available buffer through use of a pointer to the current buffer and a bit vector representing the combination of available buffers. For each pointer position, a priority encoder determines the next buffer from the available buffer bit vector. For example, if 8 buffers were to be implemented in this manner, 8 priority encoders would typically be used. The output of all the encoders is then driven to a multiplexer (mux), which uses the pointer to the current buffer to pick which encoder's output to use. Each encoder is for a different pointer value, and accordingly, cannot be shared by other pointer values.

The following truth tables correspond to an exemplary 3-buffer configuration that employs priority encoders.

Encoder 0:

Input	Output
000	000
001	001
010	010

011	010
100	100
101	100
110	010
111	010

Encoder 1:

Input	Output
000	000
001	001
010	010
011	001
100	100
101	100
110	100
111	100

Encoder 2:

Input	Output
000	000
001	001
010	010
011	001
100	100
101	001
110	010
111	001

Output Mux
(Input is current pointer and guaranteed to have one and only one bit set):

Input	Output
001	Encoder0
010	Encoder1
100	Encoder2

As the number of buffers increase, the number of input and output bits for each encoder also increases. Furthermore, this requires an increase in the size of the mux, as well. As a result, there is an almost exponential growth in the required logic as the number of buffers increase. Accordingly, an improved approach is desired.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIGURE 1 is a block diagram illustrating the inputs and outputs of a computational cell implemented by the present invention;

FIGURE 2 is a block schematic diagram illustrating a cascaded array of computational cells in accord with an exemplary embodiment of the invention;

FIGURE 3 is a detailed schematic diagram illustrating a set of logic gates employed in a exemplary embodiment of the computational cell;

FIGURE 4 is a block schematic diagram in accord with FIGURE 2 illustrating the logic values at each of the inputs and outputs of the logic circuits in the array of computational cells under a predefined starting condition; and

FIGURE 5 is a block schematic diagram of a processor that includes an array of buffers that are allocated through use of the array of computational cells an accord with the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

The present invention comprises circuitry that enables selection of the next available entry in an array of buffers based on an available vector and a current selected entry vector. In general, buffers within an array of some quantity of buffers are desired to be accessed by devices such as microprocessors for temporary storage of data. The actual quantity of buffers that may be accessed through implementation of the present invention, as described below, is not limited. For convenience, the quantity of buffers will be denoted as *b* buffers, since the invention is extendible to any value of b > 1 buffers.

In one embodiment, the circuitry comprises a quantity of computational cells that are organized such that there is a one-to-one correspondence to respective buffers among the quantity of buffers that are desired to be accessed (i.e., the quantity of computational cells is equal to the quantify of buffers (= *b*)). With reference to FIGURES 1-4, each computational cell is denoted by *Cx*, wherein x is in the range of 0 to *b*-1. As shown in FIGURE 1, each computational cell *Cx* has 3 inputs, denoted *Ax*, *Px*, and *Ix*, and two outputs, denoted *0x* and *Nx*, and includes combinational logic to calculate each of the 2 outputs and 3 inputs. FIGURE 2 illustrates an exemplary buffer allocation circuit 10 comprising an array of 8 computational cells Cx coupled together in a cascaded fashion, wherein each computation cell receives input data and provides output data corresponding to a respective buffer Bx (i.e., B[0], B[1], etc.), in a buffer array 12.

The inputs *Ax*, *Px*, and *Ix* to the array of computational cells are defined as follows. The *Ax* inputs collectively define an availability vector consisting of 1 bit for each buffer (i.e., 1 bit for each computational cell *Cx*). Each bit is asserted (i.e., 1) when a buffer is available for use and de-asserted (i.e., 0) if the buffer is being used. Each bit of the availability vector is connected to a corresponding *Ax* input. The *Px*

inputs collectively define a current selected entry vector consisting of 1 bit for each buffer. One bit is asserted at a time in the selected entry vector, indicating which entry or buffer was the last to be selected. Each bit of this selected entry vector is connected to a corresponding *Px* input. As shown in FIGURE 2, The *Ix* inputs are connected to a respective *Ox* output from a preceding (i.e., adjacent) cell. For example, the I(1) input is connected to the O(0) output, the I(2) input is connected to the O(1) output, etc. In addition, the I(0) input is connected to the O(*b*-1) output.

Outputs *Ox* and *Nx* from the array of computational cells are as follows. The *Nx* outputs form a next availability vector consisting of 1 bit from each computational cell, wherein each bit is connected to a corresponding *Nx* output. Only 1 bit is asserted at any one time, wherein the asserted bit represents the next selected entry. The *Ox* outputs are connected to the *Ix* inputs of the next cell (i.e., the cell to the immediate left), and comprise logic values based on the equations defined below.

Each computational cell *Cx* includes logic to implement the following logic equations:

$$N = A \text{ AND } I \quad (1)$$

$$O = P \text{ OR } (\text{NOT } A \text{ AND } I) \quad (2)$$

An exemplary logic circuit 14 for implementing the foregoing logic equations is shown in FIGURE 3, and includes a pair of AND gates 16 and 18, an inverter 20, and an OR gate 22. AND gate 16 produces an *Nx* output by logically ANDING *Ax* and *Ix* inputs. AND gate 18 produces an output 24 by logically ANDING the *Ix* input and an inverted *Ax* input, which is inverted by inverter 20. Output 24 of AND gate 18 is then logically OR'ed with input *Px* (by OR gate 22) to produce output *Ox*. As will be recognized by those skilled in the art, other logic circuit components may be implemented to produce similar outputs in accord with equations (1) and (2).

With reference to FIGURE 4, an exemplary data configuration corresponding to a current usage of buffers B[0] – B[7] in buffer array 12 is illustrated, wherein buffers B[0] and B[1] are in current use, and buffer B[1] is the current selected buffer. Accordingly, the *Ax* data is defined by an available vector 26 with a value of [11111100], indicating that buffers B[0] and B[1] are currently in use, while buffers B[2] – B[7] are available. Furthermore, the *Px* data collectively comprises a current selected entry vector 28 with a value of [00000010], indicating that buffer B[1] is the currently selected buffer, and the *Nx* data collectively comprise a next available vector 30 with a value of [00000100], indicating that the next available buffer is B[2]. Once buffer B[2] is allocated for use, the value of available vector 26 will change to [11111000], the value of selected entry vector 28 will change to [00000100], and the value of next available vector 30 will change to [00001000], indicating the buffer B[3] is the next available buffer.

The present invention may be implemented in various logic devices, such as a processor 32 shown in FIGURE 5. Processor 32 includes a buffer allocation circuit 34 that is substantially similar to buffer allocation circuit 10, which is used to allocate buffers from among an array of buffers 36. In addition, processor 32 includes typically processing circuitry, such as functional units, cache, etc., (all not shown).

The above description of illustrated embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific embodiments of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize.

Although the present invention has been described in connection with a preferred form of practicing it and modifications thereto, those of ordinary skill in the

art will understand that many other modifications can be made to the invention within the scope of the claims that follow. Accordingly, it is not intended that the scope of the invention in any way be limited by the above description, but instead be determined entirely by reference to the claims that follow.

CLAIMS

What is claimed is:

1. Apparatus comprising:

an array of computational cells coupled to one another and having a one-to-one correspondence with respective buffers of an array of buffers, wherein each computational cell includes:

a first input for receiving data corresponding to an availability status of the respective buffer corresponding to the computational cell;

a second input for receiving data corresponding to a currently selected buffer from among the array of buffers; and

a first output upon which data is produced for identifying a next available buffer,

wherein the data produced on the first outputs of the computational cells collectively comprise a next available buffer vector that identifies a next buffer in the buffer array to be allocated.

2. The apparatus of Claim 1, wherein each computational cell further comprises:

a third input; and

a second output coupled to the third input of a next computational cell,

wherein data is produced on the second output of a given computational cell as a function of data received at the first, second, and third inputs for the computational cell.

3. The apparatus of Claim 2, wherein each computational cell comprises:

an inverter for receiving data on the first input of the cell and having an output;

a first AND gate having a first input coupled to the output of the inverter; and a second input for receiving data on the third input of the cell, and having an output;

a second AND gate, having a first input for receiving data on the first input of the cell and a second input for receiving data on the third input of the cell, said second AND gate having an output corresponding to the first output of the cell; and

an OR gate, having a first input coupled to the output of the first and gate, and a second input for receiving the data on the second input of the cell, said OR gate having an output corresponding to the second output of the cell.

4. The apparatus of Claim 2, wherein the first input of a given computational cell is labeled A, the second input is labeled P, the third input is labeled I, the first output is labeled N, and the second output is labeled 0, and further wherein each computational cell produces a logic value at its first output N based on the logic equation,

$$N = A \text{ AND } I$$

and wherein each cell produces a logic value at its second output O based on the logic equation,

$$0 = P \text{ OR } (\text{NOT } A \text{ AND } I).$$

5. The apparatus of Claim 2, wherein a plurality of computational cells are arranged in a cascaded order so as to define 0^{th} to N^{th} computational cells such that the second output from an i^{th} computational cell is coupled to the third input of an (i^{th} + 1) computational cell, and the second output from the N^{th} computational cell is coupled to the third input of the 0^{th} computational cell.

6. The apparatus of Claim 1, wherein the array of buffers comprises N buffers and data received at the first input of each computational cell collectively comprise an availability vector comprising N bits, each bit corresponding to an availability status of a respective buffer.

7. The apparatus of Claim 10, wherein the array of buffers comprises N buffers and data received at the second input of each computational cell collectively comprise a current selected entry vector comprising N bits, each bit corresponding to a respective buffer, said current selected entry vector including only one bit that is asserted, said asserted bit identifying a most recently allocated buffer.

8. The apparatus of Claim 1, wherein the array of buffers comprises N buffers and the next available buffer vector comprises N bits, each bit corresponding to a respective buffer, said next available buffer vector including only one bit that is asserted, said asserted bit identifying the next available buffer to be allocated.

9. A processor comprising:

an array of buffers;

an array of computational cells coupled to one another in a cascaded fashion, each computational cell corresponding to a respective buffer in the array of buffers and including:

a first input for receiving data corresponding to an availability status of a buffer corresponding to the computational cell;

a second input for receiving data corresponding to a currently selected buffer from among the array of buffers;

a first output upon which data is produced for identifying a next available buffer,

a second output; and

a third input, coupled to the second output of a preceding computational cell,

wherein the data produced on the first outputs of the computational cells collectively comprise a next available buffer vector that identifies the next buffer in the buffer array to be allocated for use.

10. The processor of Claim 9, wherein said array of computational cells define 0^{th} to N^{th} computational cells, and the second output from the N^{th} computational cell is coupled to the third input of the 0^{th} computational cell.

11. The processor of Claim 2, wherein each computational cell comprises:

an inverter for receiving data on the first input of the cell and having an output;

a first AND gate having a first input coupled to the output of the inverter; and a second input for receiving data on the third input of the cell, and having an output;

a second AND gate, having a first input for receiving data on the first input of the cell and a second input for receiving data on the third input of the cell, said second AND gate having an output corresponding to the first output of the cell; and

an OR gate, having a first input coupled to the output of the first and gate, and a second input for receiving the data on the second input of the cell, said OR gate having an output corresponding to the second output of the cell.

12. The processor of Claim 9, wherein the first input of a given computational cell is labeled A, the second input is labeled P, the third input is labeled I, the first output is labeled N, and the second output is labeled 0, and further wherein each computational cell produces a logic value at its first output N based on the logic equation,

$$N = A \text{ AND } I$$

and wherein each cell produces a logic value at its second output O based on the logic equation,

$$0 = P \text{ OR } (\text{NOT } A \text{ AND } I).$$

13. A method comprising:

determining an availability vector corresponding to an availability status of buffers in an array of buffers;

determining a current selected entry vector that identifies a most recently allocated buffer; and

determining a next available buffer vector that identifies the next available buffer to be allocated from among the plurality of buffers as a function of the availability vector and the current selected entry vector.

14. The method of Claim 13, wherein the array of buffers comprises N buffers and the availability vector comprises N bits, each bit corresponding to an availability status of a respective buffer.

15. The method of Claim 13, wherein the array of buffers comprises N buffers and the current selected entry vector comprises N bits, each bit corresponding to a

respective buffer, said current selected entry vector including only one bit that is asserted, said asserted bit identifying a most recently allocated buffer.

16. The method of Claim 13, wherein the array of buffers comprises N buffers and the next available buffer vector comprises N bits, each bit corresponding to a respective buffer, said next available buffer vector including only one bit that is asserted, said asserted bit identifying a next available buffer to be allocated.

BUFFER ALLOCATION CIRCUIT

ABSTRACT OF THE DISCLOSURE

An apparatus and method for selecting a next available buffer from among an array of buffers using a reduced count of logic gates. The apparatus includes an array of computational cells coupled to one another in a cascaded fashion, wherein each computational cell corresponds to a respective buffer in the array of buffers. The array of computational cells includes a first set of inputs for receiving data in accord with an availability vector comprising 1 bit for each buffer that identifies which buffers are available for allocation. A second set of inputs in accord with a current selected entry vector is also provided, wherein the current selected entry vector includes a single asserted bit that identifies that last buffer to be allocated. A computational cell includes logic to implement a pair of predefined logic equations, whereby a next available vector in accord with a first set of outputs on the array of computational cells. The next available vector comprises a single asserted bit that identifies a next available buffer to be allocated for use by apparatus, such as microprocessors, in which the invention is implemented.

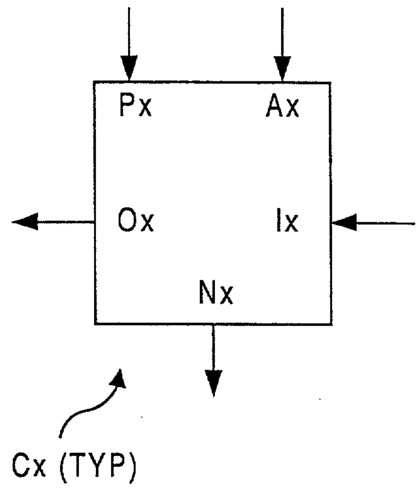
Px
Ax
Ox
Ix
Nx
Cx (TYP)

FIG. 1

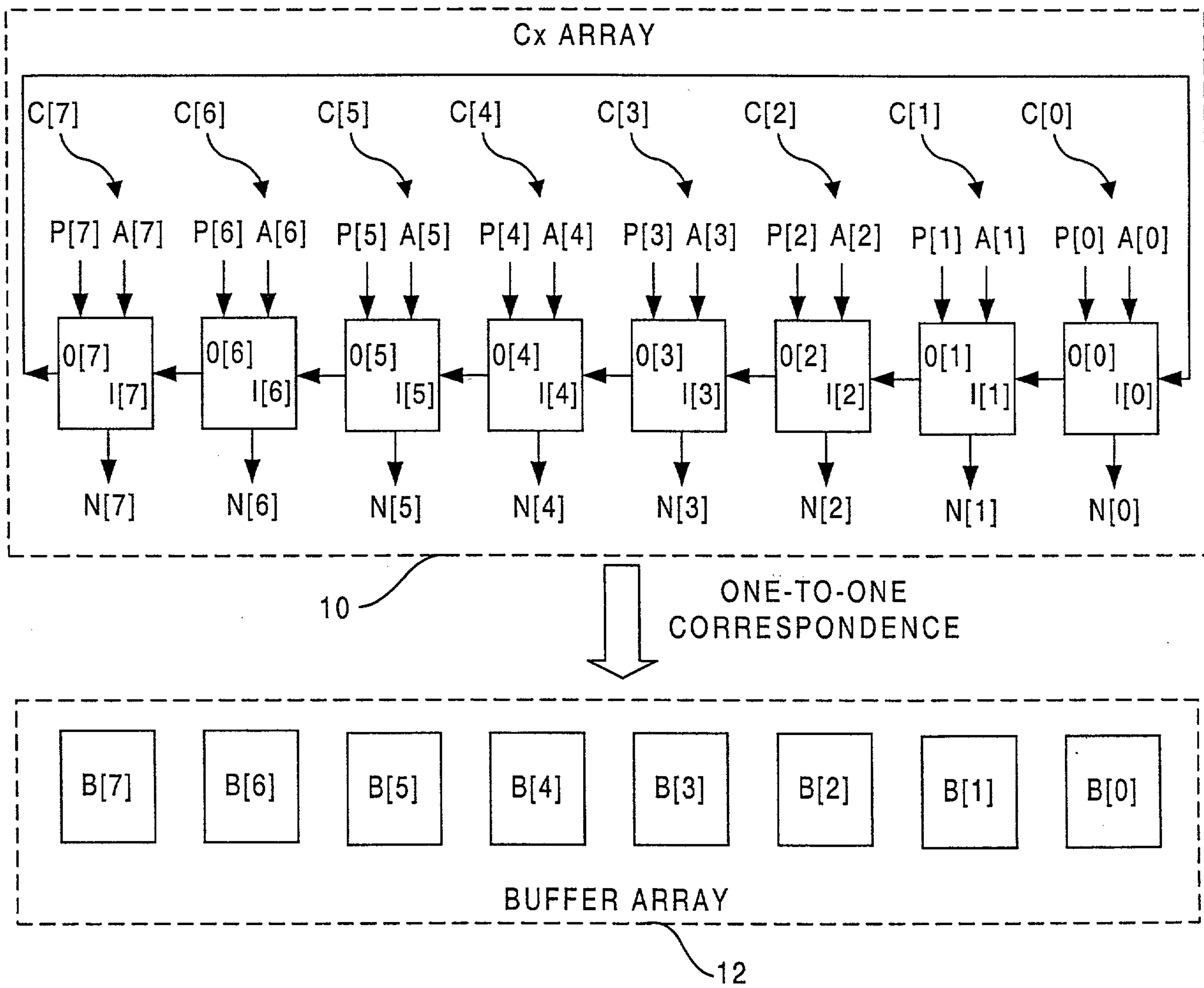
Cx ARRAY
C[7]
C[6]
C[5]
C[4]
C[3]
C[2]
C[1]
C[0]
P[7] A[7]
P[6] A[6]
P[5] A[5]
P[4] A[4]
P[3] A[3]
P[2] A[2]
P[1] A[1]
P[0] A[0]
0[7] I[7]
0[6] I[6]
0[5] I[5]
0[4] I[4]
0[3] I[3]
0[2] I[2]
0[1] I[1]
0[0] I[0]
N[7]
N[6]
N[5]
N[4]
N[3]
N[2]
N[1]
N[0]
10
ONE-TO-ONE
CORRESPONDENCE
B[7]
B[6]
B[5]
B[4]
B[3]
B[2]
B[1]
B[0]
BUFFER ARRAY
12

FIG. 2

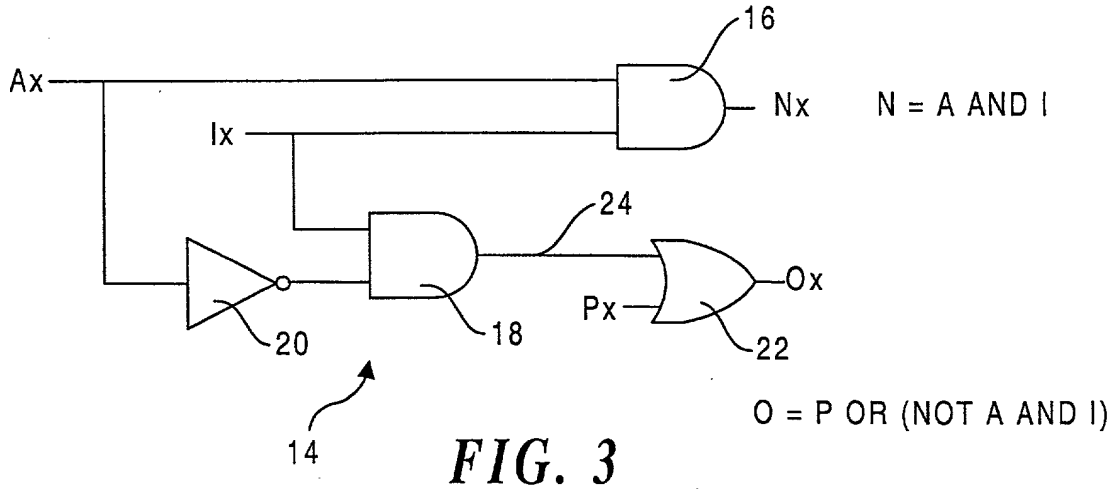
16
Ax
Nx
N = A AND I
Ix
24
Ox
Px
20
18
22
O = P OR (NOT A AND I)
14

FIG. 3

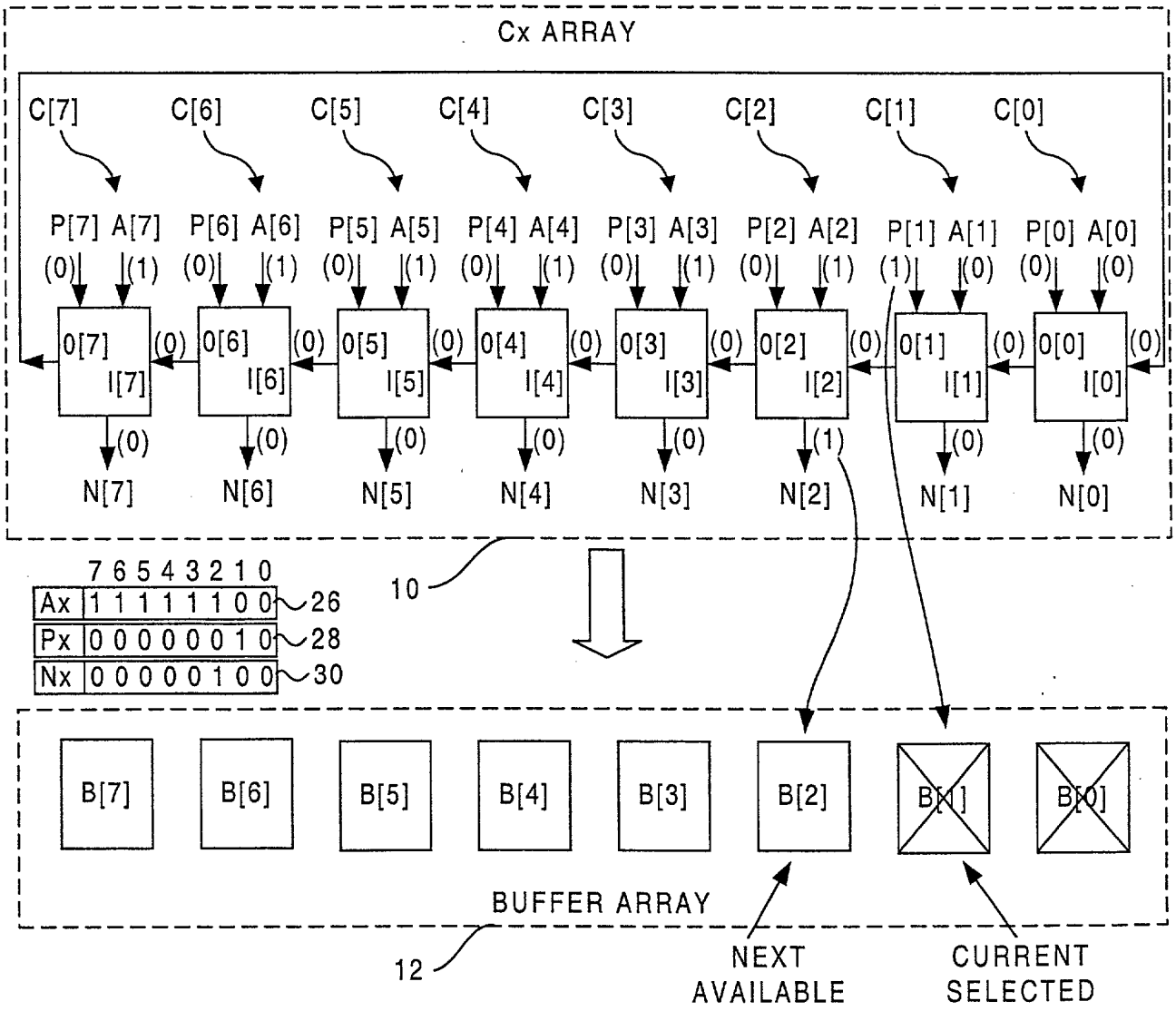
Cx ARRAY
C[7] C[6] C[5] C[4] C[3] C[2] C[1] C[0]
P[7] A[7] P[6] A[6] P[5] A[5] P[4] A[4] P[3] A[3] P[2] A[2] P[1] A[1] P[0] A[0]
O[7] I[7] O[6] I[6] O[5] I[5] O[4] I[4] O[3] I[3] O[2] I[2] O[1] I[1] O[0] I[0]
N[7] N[6] N[5] N[4] N[3] N[2] N[1] N[0]
10
7 6 5 4 3 2 1 0
Ax 1 1 1 1 1 1 0 0
Px 0 0 0 0 0 0 1 0
Nx 0 0 0 0 0 1 0 0
26
28
30
B[7] B[6] B[5] B[4] B[3] B[2] B[1] B[0]
BUFFER ARRAY
12
NEXT AVAILABLE
CURRENT SELECTED

FIG. 4

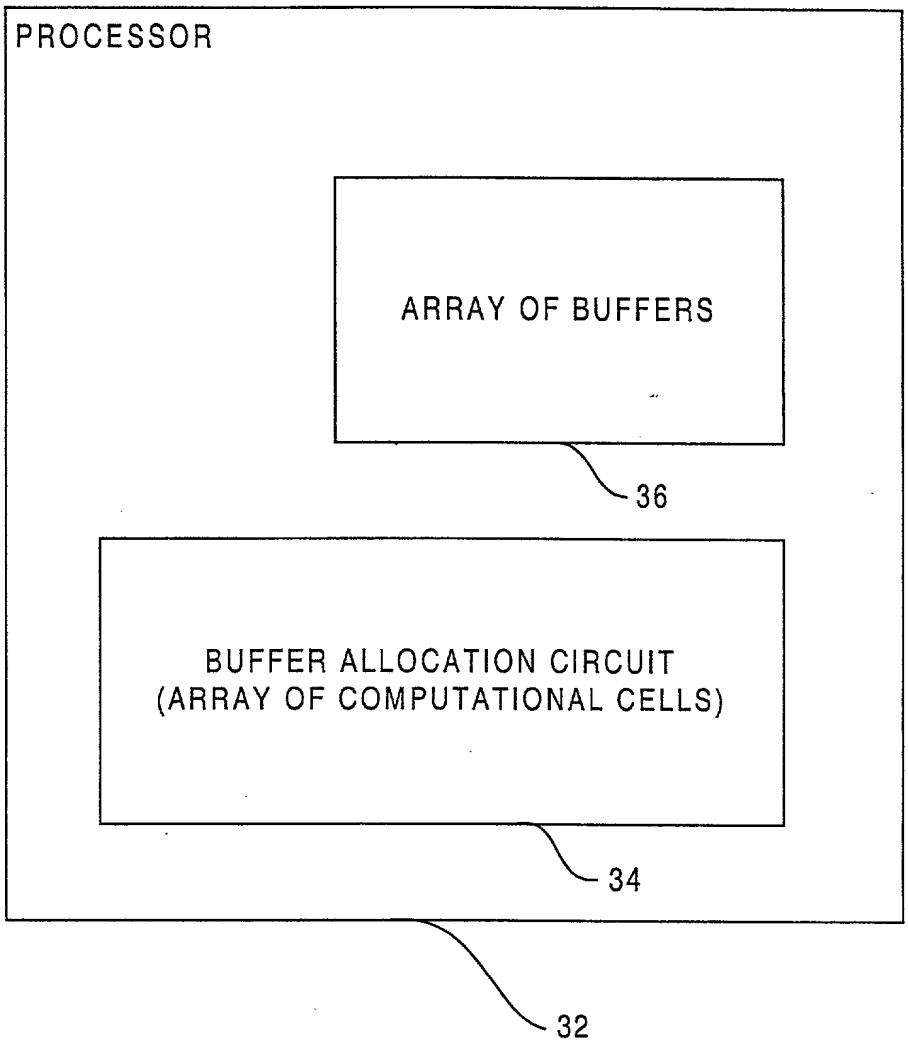
PROCESSOR
ARRAY OF BUFFERS
36
BUFFER ALLOCATION CIRCUIT
(ARRAY OF COMPUTATIONAL CELLS)
34
32

FIG. 5

Attorney's Docket No.: 042390.P8839 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
BUFFER ALLOCATION CIRCUIT

the specification of which

___ is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed: NONE

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
Number	Country	Day/Month/Year Filed	Yes	No
Number	Country	Day/Month/Year Filed	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below: NONE

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application: NONE

Application Number	Filing Date	Status -- patented, pending, abandoned
Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to R. Alan Burnett (Name of Attorney or Agent), BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to R. Alan Burnett (Name of Attorney or Agent), (425) 827-8600.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature Brian K Holscher Date 6/30/00

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APPENDIX A

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APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.